What is claimed is:

1. A multi-level flash EEPROM cell, comprising:

a tunnel oxide layer over a silicon substrate;

a floating gate over the tunnel oxide layer and electrically isolated from the silicon substrate;

a first dielectric layer over the floating gate;

a first control gate at least partially over the first dielectric layer and electrically isolated from the floating gate;

a second dielectric layer over the first control gate and covering exposed portions of the first dielectric layer;

a second control gate over the second dielectric layer and electrically isolated from the first control gate; and

a source and a drain in the semiconductor substrate, each having a sidewall aligned with a respective one of a pair of sidewalls of the second control gate.

2. The multi-level flash EEPROM cell as recited in claim 1, wherein the first and second control gates each at least partially overlap the floating gate.

3. A multi-level flash EEPROM cell, comprising:

a tunnel oxide layer over a silicon substrate;

a floating gate over the tunnel oxide layer and electrically isolated from the silicon substrate;

a dielectric layer over the floating gate;

first and second control gates at least partially over the dielectric layer and at least partially laterally positioned with respect to one another, said first and second control gates electrically isolated from the floating gate; and

a source and a drain in the substrate, each having a sidewall aligned with a respective one of a pair of sidewalls of the second control gate,

wherein the floating gate is programmable through a thermion implantation process using a voltage difference between the source and drain, and is erasable by a F-N tunneling process using a voltage difference between the first and second control gates and the drain.

4. A multi-level flash EEPROM cell in which electrons are implanted into a floating gate in a multi-level manner, control gates being electrically isolated from one another by a dielectric layer and each at least partially overlapping the floating gate to adjust electrical coupling therebetween whereby the electrons are directly implanted into or emitted from each level of the cell instead of moving from a lower level to a high level of the cell.

5. A method for manufacturing a flash EEPROM cell, comprising the steps of:

forming a tunnel oxide layer over a silicon substrate;

forming a floating gate by depositing a polysilicon

layer over the tunnel oxide layer;

forming a first dielectric layer over the floating gate;

forming a first control gate by depositing a polysilicon layer over the first dielectric layer;

forming a second dielectric layer covering the first control gate;

forming a second control gate by depositing a polysilicon layer over the second dielectric layer; and

forming a source and a drain in the silicon substrate by ion implantation with a self-aligned etching technique.

6. The method as recited in claim 5, wherein one sidewall of the first control gate at least partially overlaps a respective sidewall of the second control gate.